GA-8N-SLI Quad Royal Post Code Definition

AWARD Post Code Definition

POST (hex)	Description
CFh	Test CMOS R/W functionality.
C0h	Early chipset initialization: -Disable shadow RAM -Disable L2 cache (socket 7 or below) -Program basic chipset registers
C1h	1. Detect memory -Auto-detection of DRAM size, type and ECC. -Auto-detection of L2 cache (socket 7 or below) 2. PEG slots Auto-Configuration
C3h	Expand compressed BIOS code to DRAM
C5h	Call chipset hook to copy BIOS back to E000 & F000 shadow RAM.
0h1	Expand the Xgroup codes locating in physical address 1000:0
03h	Initial Superio_Early_Init switch.
05h	1. Blank out screen 2. Clear CMOS error flag
07h	1. Clear 8042 interface 2. Initialize 8042 self-test
08h	1. Test special keyboard controller for Winbond 977 series Super I/O chips. 2. Enable keyboard interface.
0Ah	1. Disable PS/2 mouse interface (optional). 2. Auto detect ports for keyboard & mouse followed by a port & interface swap (optional). 3. Reset keyboard for Winbond 977 series Super I/O chips.
0Eh	Test F000h segment shadow to see whether it is R/W-able or not. If test fails, keep beeping the speaker.
10h	Auto detect flash type to load appropriate flash R/W codes into the run time area in F000 for ESCD & DMI support.
12h	Use walking 1's algorithm to check out interface in CMOS circuitry. Also set real-time clock power status, and then check for override.

POST (hex)	Description
14h	Program chipset default values into chipset. Chipset default values are MODBINable by OEM customers.
16h	Initial Early_Init_Onboard_Generator switch.
18h	Detect CPU information including brand, SMI type (Cyrix or Intel) and CPU level (586 or 686).
1Bh	Initial interrupts vector table. If no special specified, all H/W interrupts are directed to SPURIOUS_INT_HDLR & S/W interrupts to SPURIOUS_soft_HDLR.
1Dh	Initial EARLY_PM_INIT switch.
1Fh	Load keyboard matrix (notebook platform)
21h	HPM initialization (notebook platform)
23h	1. Check validity of RTC value: e.g. a value of 5Ah is an invalid value for RTC minute. 2. Load CMOS settings into BIOS stack. If CMOS checksum fails, use default value instead. 3. Prepare BIOS resource map for PCI & PnP use. If ESCD is valid, take into consideration of the ESCD's legacy information. 4. Onboard clock generator initialization. Disable respective clock resource to empty PCI & DIMM slots. 5. Early PCI initialization: -Enumerate PCI bus number -Assign memory & I/O resource -Search for a valid VGA device & VGA BIOS, and put it into C000:0.
25h	PCI Bus Initialization
26h	Init clock Generator
27h	Initialize INT 09 buffer
29h	1. Program CPU internal MTRR (P6 & PII) for 0-640K memory address. 2. Initialize the APIC for Pentium class CPU. 3. Program early chipset according to CMOS setup. Example: onboard IDE controller. 4. Measure CPU speed
2Bh	Invoke video BIOS.
2Dh	1. Initialize multi-language 2. Put information on screen display, including Award title, CPU type, CPU speed ....
33h	Reset keyboard except Winbond 977 series Super I/O chips.
3Ch	Test 8254
3Eh	Test 8259 interrupt mask bits for channel 1.

POST (hex)	Description
40h	Test 8259 interrupt mask bits for channel 2.
43h	Test 8259 functionality.
47h	Initialize EISA slot
49h	1. Calculate total memory by testing the last double word of each 64K page. 2. Program write allocation for AMD K5 CPU.
4Eh	1. Program MTRR of M1 CPU 2. Initialize L2 cache for P6 class CPU & program CPU with proper cacheable range. 3. Initialize the APIC for P6 class CPU. 4. On MP platform, adjust the cacheable range to smaller one in case the cacheable ranges between each CPU are not identical.
50h	Initialize USB
52h	Test all memory (clear all extended memory to 0)
55h	Display number of processors (multi-processor platform)
57h	1. Display PnP logo 2. Early ISA PnP initialization -Assign CSN to every ISA PnP device.
59h	Initialize the combined Trend Anti-Virus code.
5Bh	(Optional Feature) Show message for entering AWDFLASH.EXE from FDD (optional)
5Dh	1. Initialize Init_Onboard_Super_IO switch. 2. Initialize Init_Onbaord_AUDIO switch.
60h	Okay to enter Setup utility; i.e. not until this POST stage can users enter the CMOS setup utility.
65h	Initialize PS/2 Mouse
67h	Prepare memory size information for function call: INT 15h ax=E820h
69h	Turn on L2 cache
6Bh	Program chipset registers according to items described in Setup & Auto-configuration table.
6Dh	1. Assign resources to all ISA PnP devices. 2. Auto assign ports to onboard COM ports if the corresponding item in Setup is set to "AUTO".
6Fh	1. Initialize floppy controller 2. Set up floppy related fields in 40:hardware.
73h	(Optional Feature) Enter AWDFLASH.EXE if : -AWDFLASH is found in floppy drive.

POST (hex)	Description
	-ALT+F2 is pressed
75h	Detect & install all IDE devices: HDD, LS120, ZIP, CDROM.....
77h	Detect serial ports & parallel ports.
7Ah	Detect & install co-processor
7Fh	1. Switch back to text mode if full screen logo is supported. -If errors occur, report errors & wait for keys -If no errors occur or F1 key is pressed to continue: ◆Clear EPA or customization logo.
E8POST.ASM starts	
82h	1. Call chipset power management hook. 2. Recover the text fond used by EPA logo (not for full screen logo) 3. If password is set, ask for password.
83h	Save all data in stack back to CMOS
84h	Initialize ISA PnP boot devices
85h	1. USB final Initialization 2. NET PC: Build SYSID structure 3. Switch screen back to text mode 4. Set up ACPI table at top of memory. 5. Invoke ISA adapter ROMs 6. Assign IRQs to PCI devices 7. Initialize APM 8. Clear noise of IRQs.
93h	Read HDD boot sector information for Trend Anti-Virus code
94h	1. Enable L2 cache 2. Program boot up speed 3. Chipset final initialization. 4. Power management final initialization 5. Clear screen & display summary table 6. Program K6 write allocation 7. Program P6 class write combining
95h	1. Program daylight saving 2. Update keyboard LED & typematic rate
96h	1. Build MP table 2. Build & update ESCD 3. Set CMOS century to 20h or 19h 4. Load CMOS time into DOS timer tick

POST (hex)	Description
	5. Build MSIRQ routing table.
FFh	Boot attempt (INT 19h)